REMARKS

Entry of this Amendment is proper because it narrows the issues on appeal and does not require further search by the Examiner.

Applicant concurrently files herewith a petition and fee for a two-month extension of time.

Claims 1-18 remain pending in this application. Claim 1 has been amended to clearly set forth its connections. The amendment to claim 1 merely clarifies the connection of the command bus to the CPU. By definition, the command bus is connected to the CPU so as to carry commands. Thus, the amendment does not affect the scope of claim 1, and the entry of this Amendment is appropriate at this time.

Claims 1-4 and 6-18 were rejected under 35 U.S.C. §103(a) as being unpatentable over the admitted prior art (APA) in view of Virajpet et al., U.S. Patent No. 6,480,948. Claim 5 was rejected under 35 U.S.C. §103(a) as being unpatentable over the APA and Virajpet in view of Ueki et al., U.S. Patent No. 6,651,152. These rejections are respectfully traversed.

Independent Claim 1 and Its Dependent Claims 2, 3, and 13-18

Independent claim 1 recites five elements. With reference to the exemplary embodiment of Figure 2, these are a central processing unit (CPU) 2, a data bus 3, a cache 7, a command bus 5, and a memory 12. The data bus 3 is electrically connected to the CPU 2. The command bus 5 is electrically connected to the cache 7 and the CPU 2 and is separated from the data bus 3. The memory 12 is electrically connected to the command bus 5. The memory 12 stores an interruption handling routine.

The APA teaches four elements. With reference to Figure 1, these are a CPU 42, a data bus 43, a cache 47, and a command bus 45. The data bus 43 is electrically connected to the CPU 42. The command bus 45 is electrically connected to the cache 47 and the CPU and is separated from the data bus 43. As recognized in the Office Action, the APA does not show or suggest a memory electrically connected to the command bus and storing an interruption handling routine.

The Office Action contends that Virajpet "describes a memory capable of storing an interrupt code" and cites Virajpet at column 3, lines 18-26. That portion of Virajpet describes accessing an internal SRAM for interrupt vectors or interrupt code. Nevertheless, Virajpet does not disclose or suggest the memory of claim 1 and its dependent claims and does not disclose or suggest the particular connections of claim 1 and its dependent claims.

Virajpet's controller 5 includes a processor 10 coupled by an address/data/command bus 11 to a bus/memory controller 12, an SRAM internal memory 16, a ROM internal memory 18, and a peripheral device 14. Memories 16 and 18 and peripheral device 14 are connected to bus/memory controller 12 by separate "device select" lines, which are not a part of bus 11. See Virajpet at column 2, lines 53-67, column 3, lines 53-58, and Figure 1.

If the CPU of claim 1 is Virajpet's processor 10, then the data bus of claim 1 is Virajpet's address/data/command bus 11. However, claim 1 recites that the memory is electrically connected to the command bus and also states that the command bus is separated from the data bus. Virajpet teaches a single data and command (and address) bus. By teaching that the memory be connected to the bus that carries the data, as well as the addresses and the commands, Virajpet teaches away from invention of claim 1 and its

dependent claims.

Thus, a person skilled in the art would not combine Virajpet with the APA.

Even if a person skilled in the art did combine Virajpet with the APA, the result would not be the invention of claim 1 and its dependent claims, since that result would electrically connect the memory to a bus carrying data and addresses. As pointed out in the present specification at, for example, page 6, lines 12-15, the claimed invention minimizes the interruption response time.

It is accordingly submitted that independent claim 1 and its dependent claims 2, 3, and 13-18 distinguish patentably from the combination of the APA and Virajpet and are allowable.

Independent Claim 4 and Its Dependent Claims 5-12

Independent claim 4 recites eight elements. With reference again to the exemplary embodiment of Figure 2, these are a first bus 3, a second bus 5, a third bus 6, a fourth bus 10, a CPU 2, a bus controller 4, a command cache 7, and a command memory 12. The bus controller 4 is connected to the CPU 2 through the first bus 3. The command cache 7 is electrically connected to the CPU 2 through the second bus 5 and to the bus controller through the third bus 6. The command memory 12 is electrically connected to the second bus 5 through the fourth bus 10. The command memory 12 stores an interruption handling routine.

The APA teaches 6 elements. With reference to Figure 1, these are a first bus 43, a second bus 45, a third bus 46, a CPU 42, a bus controller 44, and a command cache 47. As

recognized in the Office Action, the APA does not show or suggest a fourth bus and a command memory electrically connected to the second bus through the fourth bus.

The Office Action contends that Virajpet "describes the connection of the internal memory (Fig 1:#16) to the CPU (Fig 1: #10) as shown in Fig 1." The Office Action further contends that this would "allow a direct path to the CPU, thus allowing a quick access to the interrupt code" and cites Virajpet at column 3, lines 23-28. That portion of Virajpet describes accessing an internal SRAM for interrupt vectors or interrupt code and indicates that such access will be "relatively fast." Nevertheless, Virajpet does not disclose or suggest the memory of claim 4 and its dependent claims and does not disclose or suggest the particular connections of claim 4 and its dependent claims.

As set forth above, Virajpet's controller 5 includes a processor 10 coupled by an address/data/command (or first) bus 11 to a bus/memory controller 12, an SRAM internal memory 16, a ROM internal memory 18, and a peripheral device 14. Memories 16 and 18 and peripheral device 14 are connected to bus/memory controller 12 by separate "device select" lines (or second, third, and fourth buses). See Virajpet at column 2, lines 53-67, column 3, lines 53-58, and Figure 1.

If the CPU of claim 4 is Virajpet's processor 10 and the bus controller of claim 4 is Virajpet's bus/memory controller 12, then the first bus of claim 4 is Virajpet's address/data/command bus 11.

If Virajpet's internal memory (ROM) 18 is the cache of claim 4, then the third bus is the device select line connecting memory 18 to controller 12. However, the second bus of claim 4 would then be bus 11 - - the same as the first bus of claim 4.

In addition, if Virajpet's internal memory (SRAM) 16 is the command memory of claim 4, as contended in the Office Action, then Virajpet does not have the claimed fourth bus by which the command memory is electrically connected to the "second" bus (which is the first bus).

Again, Virajpet teaches away from invention of claim 4 and its dependent claims. Thus, a person skilled in the art would not combine Virajpet with the APA. Even if a person skilled in the art did combine Virajpet with the APA, the result would not be the invention of claim 4 and its dependent claims, since that result would electrically connect the memory to a bus carrying data and addresses. As pointed out in the present specification at, for example, page 6, lines 12-15, the claimed invention minimizes the interruption response time.

It is accordingly submitted that independent claim 4 and its dependent claims 5-12 distinguish patentably from the combination of the APA and Virajpet and are allowable.

Dependent Claims 8, 10, 15, and 17

Dependent claims 8, 10, 15, and 17 add to their respective parent claims an external terminal electrically connected to the CPU. This is terminal 13 depicted in Figure 1 and described in the specification at page 7, lines 20-21 and page 8, line 26. The Office Action contends that Virajpet teaches such an external terminal, and cites Virajpet at column 4, lines 5-14. However, Virajpet's external terminal is connected to his bus/memory controller 12, not his processor 10. See Virajpet at column 4, lines 7-9 and Figure 1. An external terminal having such a connection would perform a wholly different function from those recited in claims 8, 10, 15, and 17. It is accordingly submitted that claims 8, 10, 15, and 17 are

allowable for this further reason.

The Specification

The Office Action objected to the specification with the contention that it does not describe element 13 in Figure 2. Element 13 is the "external terminal" described on page 7, lines 20-21 of the specification. Note that it is also mentioned at page 8, line 26. By the above amendment, the reference numeral 13 has been added to the page 7 mention of the external terminal.

Conclusion

In view of the foregoing, Applicant submits that claims 1-18, all the claims presently pending in the application, are patentably distinct over the prior art of record and are allowable, and that the application is in condition for allowance. Such action would be appreciated.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned attorney at the local telephone number listed below to discuss any other changes deemed necessary for allowance in a telephonic or personal interview.

To the extent necessary, Applicant petitions for an extension of time under 37 CFR §1.136. The Commissioner is authorized to charge any deficiency in fees, including

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extension of time fees, or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

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